**AMENDMENTS TO THE DRAWINGS**:

Applicants propose amending "-0.5 -0.3 -0.1 0.1 0.3 0.5 -0.4 -0.2 0 0.2 0.4" in FIG. 6 to instead be "0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0", to overcome the objection.

Approval is respectfully requested.

## REMARKS/ARGUMENT

Figure 6 has been amended to correct the x-axis numbers. Accordingly, the objection to the drawings is overcome.

The specification has been amended to overcome Examiner's objections to the specification.

Claims 9, 14 and 16 have been amended to overcome the informalities identified by Examiner. Regarding Claim 9, the phrase: "the ratio of the rotating capacitor to the sum of the rotating capacitor and history capacitor" is precise. However, since the ratio of CR to CH is typically very small, on the order of 1:100, it is equivalent from a practical engineering standpoint to talk about CR to CH ratio alone. For example, if CR/CH = 0.01 then CR/(CH+CR) = 0.0099, i.e., only 1% of error, which is insignificant. Therefore, to clarify, the word "substantially" has been added to Claim 9. Accordingly, the objections to Claims 9, 14 and 16 are overcome.

Claim 14, indicated as being allowable if rewritten or amended to include the limitations of the base claim and any intervening claims, is in independent form. Accordingly, Claim 14 stands allowable.

1) Claim 2 stands rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Applicants respectfully traverse this rejection as follows:

Claim 2 is almost identical to Claim 3, except for the Claim 3 limitation of four quadrature LO phases (ILO+, QLO+, ILO- and QLO- in Figure 1 or LO I+, LO Q+, LO I- and LO Q- in Figure 3) and the term of "consist of". Claim 2, as amended, has a limitation of at least two quadrature phases (term of "comprise two phases"). Hence, Claim 2 uses the subset of clock phases of Claim 3. It is well known in the art that only two quadrature phases (in-phase and quadrature-phase) are needed for the quadrature mixing. In practice, however, four phases are used due to the additional benefits of differential or pseudo-differential circuit topology. Just to demonstrate the wide use of two quadrature phases as a subset of four phases, inspection of Figure 3 in Mole (cited by the Examiner) reveals only two LO 48 phases: 0 and 90 degrees. However, Figure 4 shows four phases: I, Q, -I, -Q. Accordingly, the 35 U.S.C. 112 rejection is overcome.

2) Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Mole et al. (US 6,226,509). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 1-3 be sustainable, it is fundamental that "each and every element as set forth in the claims be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1 requires and positively recites, a method for complex image rejection filtering in a **direct sampling mixer** comprising the steps of: "**sampling an RF input** with multiple phases of a local oscillator clock, each of the local oscillator phases **producing a discrete-time signal stream**" and "processing the multiple phases of the discrete-time signal in multiple paths, the paths sharing among themselves the discrete-time samples, whereby a bandpass filter characteristic is achieved during the processing step, and whereby an RF image is substantially rejected".

In contrast, Mole teaches an image-reject mixer operating in the continuous-time domain and producing continuous-time output waveform. This is completely different from the mixer of the claimed invention that operates in the discrete-time domain and produces discrete-time output samples.

Specifically, Mole does not teach or suggest the following limitations required by Claim 1:

1. "**direct sampling mixer**" as recited in the preamble. The mixer uses a conventional continuous-time mixing. The shunt capacitor 86 and load resistance RL in Figure 4 provide low pass filtering to remove the high-frequency mixing terms and only pass the baseband or IF components. It should be noted that the term "direct sampling mixer" is commonly accepted in the RF community and which specifically does not include the mixer described in Mole.
2. "**sampling an RF input**" – the RF input is simply down-converted to an intermediate frequency (IF) output through a continuous-time operation. Mole does not teach sampling of an RF waveform. Mole, however, teaches sampling of an IF signal for the purpose of A/D conversion, but that operation is irrelevant for RF mixing.
3. "local oscillator phases **producing a discrete-time signal stream**" – The output is a typical continuous-time waveform, not discrete-time.

Accordingly, the 35 U.S.C. 102(b) rejection of Claim 1 is improper and must be withdrawn.

Claims 2 & 3 stand allowable as depending from allowable Claim 1 and including further limitations not taught or suggested by the references of record.

Claim 2 further defines the method according to claim 1 wherein the multiple phases of the local oscillator clock comprise atleast two phases I and Q spaced approximately 90 degrees apart. Claim 2 stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 3 further defines the method according to claim 1 wherein the multiple phases of the local oscillator clock consist of four phases I+, I-, Q+, Q-, spaced approximately 90 degrees apart. Claim 3 stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

3) Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mole et al. (US 6,226,509) in view of Hunsinger et al. (US 5,465,396). Applicants respectfully traverse this rejection as set forth below.

Claim 4 further defines the method according to claim 1 wherein the discrete-time signal stream comprises charge packets. Claim 4 stands allowable for the same reasons set forth above in support of the allowability of Claim 1. Whatever else Hunsinger teaches, it does not teach the previously described deficiency of Mole. Further, and contrary to the Examiner assertion, it is not obvious how to combine the acoustic charge transport (ACT) charge-packet operating device in Hunsinger with the continuous-time mixer in Mole. Combining the two disparate domains would be extremely challenging and would not work. Accordingly, no prima facie case of obviousness has been established for Claim 4.

Claim 5 further defines the method according to claim 1 wherein the step of sharing discrete-time samples further comprises the sharing of charge packets. Claim 5 stands allowable for the same reasons set forth above in support of the allowability of Claim 1. Whatever else Hunsinger teaches, it does not teach the previously described deficiency of Mole. Further, and contrary to Examiner's assertion, Mole does not teach "sharing of charge packets". There are simply no charge packets to start with. Moreover, Examiner has failed to identify where such teaching occurs in the reference. Accordingly, no prima facie case of obviousness has been established for Claim 5.

Claim 6 further defines the method according to claim 1 further comprising the step of converting an RF input voltage into current. Claim 6 stands allowable for the same reasons set forth above in support of the allowability of Claim 1. Accordingly, no prima facie case of obviousness has been established for Claim 6.

Claim 7 requires and positively recites, a method for complex filtering in a **direct sampling mixer** comprising: "**sampling an RF input** with I and Q phases of a local oscillator clock, each of the phases **producing a stream of charge packets**", "processing the I and Q charge packets in separate signal processing paths" and "**sharing the I and Q charge packets** between the signal processing paths, whereby a bandpass filter characteristic is achieved during the processing step, and whereby an RF image is substantially rejected".

In contrast, Mole teaches an image-reject mixer operating in the continuous-time domain and producing continuous-time output waveform. This is completely different from the mixer of the claimed invention that operates in the discrete-time domain and produces discrete-time output samples.

Specifically, Mole does not teach or suggest the following limitations required by Claim 7:

4. "**direct sampling mixer**" as recited in the preamble. The mixer uses a conventional continuous-time mixing. The shunt capacitor 86 and load resistance RL in Figure 4 provide low pass filtering to remove the high-frequency mixing terms and only pass the baseband or IF components. It should be noted that the term "direct sampling mixer" is commonly accepted in the RF community and which specifically does not include the mixer described in Mole.
5. "**sampling an RF input**" – the RF input is simply down-converted to an intermediate frequency (IF) output through a continuous-time operation. Mole does not teach sampling of an RF waveform. Mole, however, teaches sampling of an IF signal for the purpose of A/D conversion, but that operation is irrelevant for RF mixing.

Whatever else Hunsinger teaches, it does not teach the previously described deficiency of Mole. Further, and contrary to the Examiner assertion, it is not obvious how to combine the acoustic charge transport (ACT) charge-packet operating device in Hunsinger with the continuous-time mixer in Mole. Combining the two disparate domains would be extremely challenging and would not work. Accordingly, no prima facie case of obviousness has been established for Claim 7.

Moreover, even had the Examiner considered all of the words of Claims 4-7, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

4) Claims 8-13 and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mole et al. (US 6,226,509) in view of Staszewski et al. (US 20030035499). Applicants respectfully traverse this rejection as set forth below.

Independent Claim 8 requires and positively recites, a complex filter system for filtering a high frequency input signal, the complex filter comprising: "a **first IIR filter** for sampling an I+ phase of the input signal", "a **second IIR filter** for sampling an I- phase of the input signal", "a **third IIR filter** for sampling an Q+ phase of the input signal", "a **fourth IIR filter** for sampling an Q- phase of the input signal", and "**wherein the IIR filters are interconnected for rotation** of filtered signals such that in combination the interconnected IIR filters provide a complex filter".

Mole does not teach or suggest "a first IIR filter for sampling I+ phase of the input signal", as well as three other similar limitations ("second", "third" and "fourth" "IIR filter" ...). Examiner admits that there is no teaching of IIR filters in Mole (Office Action, page 8, line 8). To cure this shortcoming, the Examiner offers Staszewski.

Applicants first point out that Mole further does not teach or suggest "wherein the IIR filters are interconnected for rotation". There is no "rotation" in Mole. Moreover, the IIR filter type disclosed in Staszewski is applicable to discrete-time operation whereas Mole teaches only continuous-time operation. Accordingly, combing Staszewski with Mole will not work due to the entirely different mode of operations (discrete-time versus continuous-time). Accordingly, Mole and Staszewski are not in the same field of endeavor and any purported combination of the two will not operate as suggested by Examiner. Accordingly, the 35 USC 103(a) rejection of Claim 8 is improper and must be withdrawn.

Claim 9 further defines a complex filter system for filtering a high frequency input signal according to claim 8 wherein each IIR filter further comprises "a history capacitor, rotating capacitor, and buffer capacitor adapted for sampling, storing and transferring charge from the input signal" and "wherein each IIR filter has a pole substantially determined by the ratio of its rotating capacitor to its history capacitor and is adapted to provide filtering of an input signal". Claim 9 stands allowable for the same reasons provided above in support of the allowance of Claim 8. In addition, it is not possible to combine the discrete-time specific constructs, such as a history capacitor, rotating capacitor and buffer capacitor into the continuous-time based mixer in Mole. Accordingly, the 35 USC 103(a) rejection of Claim 9 is improper and must be withdrawn.

Claim 10 further defines a complex filter system for filtering a high frequency input signal comprising two or more complex filter stages according to claim 8 coupled in a cascading configuration for providing high order filtering. Claim 10 stands allowable for the same reasons provided above in support of the allowance of Claim 8. Cascading filters in continuous-time domain is extremely difficult, unlike in the digital domain. The signal flow is bidirectional and the sourcing (previous) and loading

(following) stages affect the transfer function. Accordingly, the 35 USC 103(a) rejection of Claim 10 is improper and must be withdrawn.

Claim 11 further defines a complex filter system according to claim 10 further comprising one or more transconductive elements coupled between adjacent stages. Claim 11 stands allowable for the same reasons provided above in support of the allowance of Claim 10. Further, Figure 4 in Mole shows only one stage and no cascading of stages. Accordingly, the 35 USC 103(a) rejection of Claim 11 is improper and must be withdrawn.

Claim 12 further defines a complex filter system according to claim 10 further comprising one or more amplifier elements coupled between adjacent stages. Claim 12 stands allowable for the same reasons provided above in support of the allowance of Claim 10. Further, Figure 4 in Mole shows only one stage and no cascading of stages. Accordingly, the 35 USC 103(a) rejection of Claim 12 is improper and must be withdrawn.

Claim 13 further defines a complex filter system according to claim 10 further comprising one or more buffer elements coupled between adjacent stages. Claim 13 stands allowable for the same reasons provided above in support of the allowance of Claim 10. Further, Figure 4 in Mole shows only one stage and no cascading of stages. Accordingly, the 35 USC 103(a) rejection of Claim 13 is improper and must be withdrawn.

Claim 15 further defines a complex filter system according to claim 8 wherein the complex filter comprises a loop filter in a sigma-delta analog-to-digital converter. Claim 15 stands allowable for the same reasons provided above in support of the allowance of Claim 8. It would be extremely challenging and non-obvious to combine sigma-delta

ADC as taught by Staszewski into Mole. Again, sigma-delta ADC would produce discrete-samples which could not be readily integrated into the continuous-time mixer in Mole. Accordingly, the 35 USC 103(a) rejection of Claim 15 is improper and must be withdrawn.

Independent Claim 16 requires and positively recites, a circuit for image rejection filtering in **a direct sampling mixer** comprising: "an input node", "four parallel output nodes for producing four phases of an output signal", "coupled to the input node, **multiple IIR filters**, each filter further comprising: a **buffer capacitor** for buffering input current; rotating capacitors coupled to the buffer capacitors in a configuration for reading the phase signal components **in rotation** and for providing mixed filtered phase signal component outputs to the output nodes".

Examiner admits that Mole fails to teach or suggest an IIR filter (Office action, page 10, line17). To cure this shortcoming, the Examiner offers Staszewski.

In addition to the above deficiency of Mole identified by Examiner, Applicants further submit that Mole fails to teach or suggest a "**direct sampling mixer**". Examiner has not identified any such teaching in Mole. Applicants further point out that there is no "rotation" in Mole. Moreover, the IIR filter type disclosed in Staszewski is applicable to discrete-time operation whereas Mole teaches only continuous-time operation. Accordingly, combing Staszewski with Mole will not work due to the entirely different mode of operations (discrete-time versus continuous-time). Accordingly, Mole and Staszewski are not in the same field of endeavor and any purported combination of the two will not operate as suggested by Examiner. Accordingly, the 35 USC 103(a) rejection of Claim 16 is improper and must be withdrawn.

Claim 17 further defines a circuit according to claim 16 wherein the direct sampling mixer comprises a sigma-delta analog-to-digital converter. Claim 17 stands allowable for the same reasons provided above in support of the allowance of Claim 16. It would be extremely challenging and non-obvious to combine sigma-delta ADC as taught by Staszewski into Mole. Again, sigma-delta ADC would produce discrete-samples which could not be readily integrated into the continuous-time mixer in Mole. Accordingly, the 35 USC 103(a) rejection of Claim 17 is improper and must be withdrawn.

Claim 18 further defines a circuit for image rejection filtering in a direct sampling mixer comprising two or more circuit stages according to claim 16 coupled in a cascaded configuration. Claim 18 stands allowable for the same reasons provided above in support of the allowance of Claim 16. Cascading filters in continuous-time domain is extremely difficult, unlike in the digital domain. The signal flow is bidirectional and the sourcing (previous) and loading (following) stages affect the transfer function. Accordingly, the 35 USC 103(a) rejection of Claim 18 is improper and must be withdrawn.

Claim 19 further defines a circuit for image rejection filtering in a direct sampling mixer according to claim 18 further comprising one or more transconductive elements coupled between adjacent stages. Claim 19 stands allowable for the same reasons provided above in support of the allowance of Claim 18. Further, Figure 4 in Mole shows only one stage and no cascading of stages. Accordingly, the 35 USC 103(a) rejection of Claim 19 is improper and must be withdrawn.

Claim 20 further defines a circuit for image rejection filtering in a direct sampling mixer according to claim 18 further comprising one or more amplifier elements coupled between adjacent stages. Claim 20 stands allowable for the same reasons provided above in support of the allowance of Claim 18. Further, Figure 4 in Mole shows only one stage

and no cascading of stages. Accordingly, the 35 USC 103(a) rejection of Claim 20 is improper and must be withdrawn.

Claim 21 further defines a circuit for image rejection filtering in a direct sampling mixer according to claim 18 further comprising one or more buffer elements coupled between adjacent stages. Claim 21 stands allowable for the same reasons provided above in support of the allowance of Claim 18. Further, Figure 4 in Mole shows only one stage and no cascading of stages. Accordingly, the 35 USC 103(a) rejection of Claim 21 is improper and must be withdrawn.

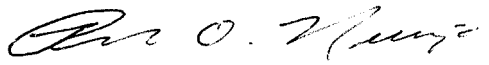
Moreover, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed**

**invention is rendered obvious**. *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Objected to Claim 14 stands allowable. Claims 1-13 and 15-21 stand allowable for the reasons set forth above. Applicants respectfully request withdrawal of the rejections and allowance of the application as the earliest possible date.

Respectfully submitted,



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